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FET GATE STRUCTURE WITH METAL GATE ELECTRODE AND SILICIDE CONTACT

Abstract

A method is provided for fabricating a single-metal or dual metal replacement gate structure for a semiconductor device; the structure includes a silicide contact to the gate region. A dummy gate structure and sacrificial gate dielectric are removed to expose a portion of the substrate; a gate dielectric is formed thereon. A metal layer is formed overlying the gate dielectric and the dielectric material. This metal layer may conveniently be a blanket metal layer covering a device wafer. A silicon layer is then formed overlying the metal layer; this layer may also be a blanket wafer. A planarization or etchback process is then performed, so that the top surface of the dielectric material is exposed while other portions of the metal layer and the silicon layer remain in the gate region and have surfaces coplanar with the top surface of the dielectric material. A silicide contact is then formed which is in contact with the metal layer in the gate region.